A High-Speed Low-Complexity Time-Multiplexing Reed-Solomon based FEC Architecture

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Abstract

A high-speed low-complexity time-multiplexing Reed-Solomon (RS)-based forward error correction (FEC) architecture based on pipelined truncated inversionless Berlekamp–Massey algorithm is presented in this paper. The proposed architecture has very high speed and very low hardware complexity compared with conventional RS-based FEC architectures. A high-throughput data rate is facilitated by employing a three-parallel processing pipelining technique and modified syndrome computation block. The time-multiplexing method for pipelined truncated inversionless Berlekamp–Massey (TiBM) architecture is used in the parallel RS decoder to reduce hardware complexity. The proposed architecture has been designed and implemented with 90-nm CMOS technology. Synthesis results show that the proposed 16-channel Reed–Solomon–based FEC architecture requires 417,600 gates and can operate at 640 MHz to achieve a throughput of 240 Gb/s. The proposed architecture can be readily applied to RS-based FEC devices for next-generation short-reach optical communications.

Keywords: RS, FEC, TiBM, optical communications, time-multiplexing.

I. Introduction

Demands for 100 Gigabit Ethernet (GbE) devices are increasing dramatically where data traffic converges, such as high performance computing, servers, data centers, and enterprise networks. In the future, bandwidth will be much more in demand than 100 GbE. For this reason, the IEEE 802.3ba task force is currently discussing the use of 40 Gb/s and 100 Gb/s Ethernet [1]. These very high speed data transmission techniques that have been developed for fiber optic networking systems have necessitated the implementation of high-speed Forward Error Correction (FEC) architecture to meet the continuing demand for even higher data rates. Also, high-speed (40 Gb/s and beyond) short-reach optical communication systems commonly use Reed–Solomon (RS) (255, 239) code [2]. The very high-speed data transmission techniques for optical communications have necessitated the implementation of high-speed low-complexity RS-based FEC architecture for even higher data rates (100 Gb/s and beyond). In this paper, we present three-parallel RS decoder architecture and high-speed low-complexity time-multiplexing RS-based FEC architecture using a truncated inversionless Berlekamp–Massey (TiBM) algorithm for next generation short-reach optical systems.

II. Three-Parallel Reed–Solomon Decoder

The RS decoder consists of three main blocks, which are: the syndrome solver (KES) block, and the Chien search and error evaluation (CSEE) block. Generally, the RS decoder can be implemented with a Berlekamp–Massey (BM) algorithm or ME algorithm to solve a key equation. In this section, we propose three-parallel RS decoder using modified syndrome computation block and pipelined TiBM (pTiBM) architecture, which provides high speed and low hardware complexity. Also, the modified syndrome computation block and CSEE block are reformulated for high data throughput three-parallel processing. The proposed three-parallel RS decoder architecture is shown in Fig. 1.
Fig. 1. Three-parallel Reed–Solomon decoder.

Fig. 2. Modified three-parallel syndrome computation block

1. Modified three-parallel syndrome computation block

The first step in the decoding algorithm is to calculate \(2t\) syndromes \(S_i(0 \leq i \leq 2t-1)\) which are used to correct fixable errors. The \(t\) is the capability of error correction. If all \(2t\) syndromes \(S_i\) \((0 \leq i \leq 2t-1)\) are zero, then the received polynomial \(R(x)\) is a valid codeword \(C(x)\), that is, no errors have occurred. The syndrome polynomial \(S(x)\) is defined as (1) and (2).

\[
S(x) = S_3x^3 + S_2x^2 + \ldots + S_x + S_0 = \sum_{i=0}^{t-1} S_{2t-1-i}x^{2t-1-i}
\]

(1)

\[
S_i = R(\alpha^i) = R_{254}\alpha^{254i} + R_{253}\alpha^{253i} + \ldots + R_{1}\alpha^i + R_0 \quad (i=0,1,2,\ldots,15)
\]

(2)

The conventional three-parallel syndrome computation block consists of \(2t\) syndrome cells, which compute the \(S_i\) value during 85 clock cycles. However, the critical path of the syndrome cell is increased if the syndrome computation block is implemented for three-parallel processing. To reduce the critical path, the syndrome polynomial can be separated into even terms and odd terms as follows:

\[
S_i(d) = R_{254}d^{254i} + R_{253}d^{253i} + \ldots + R_1d^i + R_0
\]

(3)

\[
= \bigg( R_{254}\alpha^{254i} + R_{253}\alpha^{253i} + \ldots + R_1\alpha^i + R_0 \bigg) + \bigg( R_{254}\alpha^{254i} + R_{253}\alpha^{253i} + \ldots + R_1\alpha^i + R_0 \bigg) + \ldots + \bigg( R_{254}\alpha^{254i} + R_{253}\alpha^{253i} + \ldots + R_1\alpha^i + R_0 \bigg)
\]

(4)

\[
= \sum_{i=0}^{254} \bigg( R_{254}\alpha^{254i} + R_{253}\alpha^{253i} + \ldots + R_1\alpha^i + R_0 \bigg)
\]

(5)

If the three-parallel syndrome computation block is reformulated by the syndrome polynomial shown in (6), the pipelining is possible without any additional latency. Fig. 2 shows the modified three-parallel syndrome computation block.

2. pTiBM architecture

The low-complexity TiBM architecture for a KES block was presented in our previous paper [7] and removed the unnecessary \(t-1\) PEs in the conventional RiBM architecture. Fig. 3 shows the block diagram of the proposed pTiBM architecture. In the pTiBM architecture, the original \(t+1\) PEs which are employed in the conventional RiBM architecture are used in PEs1 to PEs1 and modified \(t+1\) PEs are used in PEs2 to PEs2. Some lost zero value occurred because of truncated \(t-1\) PEs. Thus, MUX(1) and MUX(2) were added into the modified PEs2 to give zero value at the appropriate time. Also, the proposed pTiBM architecture can be pipelined for high speed. This fact represents that a time-multiplexing method can be used efficiently in the multi-channel RS-based FEC architecture. The time-multiplexing method is described in Section 4. The pTiBM architecture consists of PEs1, PEs2, and Control Units 1 and 2. Because of removed \(t-1\) PEs1, control circuits are required to adjust MUX(1) and MUX(2) in PEs2, and propagate \(\delta_i(r)\) and \(\theta_i(r)\) correctly. Control Unit 1 generates the control signal such as \(MC(r)\), \(\gamma(r)\) and \(\delta_0(r)\).

3. Pipelined three-parallel CSEE block

The CSEE block finds error locations and error values. Fig. 4 represents the three-parallel Chien search blocks and their cells. The Forney algorithm block is almost the same structure as the Chien search block, except that the C8 cell is eliminated. The dotted line in Fig. 5 is a cutline for pipelining. Then, the critical path delay of the Chien search block is reduced from \(7T_{xor} + T_{mux} + T_{ff}\) to \(3T_{xor} + T_{mux} + T_{ff}\).
4. 16-Channel Time-Multiplexing RS-based FEC Architecture

Fig. 5. shows the proposed 4-channel time-multiplexing RS-based FEC architecture and 16-channel RS-FEC architecture is made up of four 4-channel RS decoders. The syndrome computation block provides 2t syndromes after 85 clock cycles which are required for computing the syndrome polynomial. Since four syndrome computation blocks are connected by only one KES block, syndrome values are entered into the KES block alternately. The KES block outputs four error location polynomials λ(x) and four error value polynomials ω(x) in parallel after 64 clock cycles. Finally, a CSEE block completes error correction. Most conventional high-speed RS decoders have used ME algorithms to solve the KES block, because the ME algorithm can be easily implemented by fully pipelined systolic-array architecture. On the other hand, the ME architecture has very high hardware complexity compared to the BM architecture. In general, the BM algorithm is difficult to use with pipelining techniques because of their feedback loops. But if many channels are used in the TiBM architecture, the pipelining techniques can be used efficiently with time-multiplexing method. Therefore, the KES block is able to process a maximum of four independent syndrome values because the iteration period for obtaining λ(x) and ω(x) in the KES block is 16 clock cycles and the syndrome computation block used 85 clock cycles for its computation. Fig. 6 (a) and (b) show the timing chart of four independent syndrome conventional ME architecture and the proposed pTiBM architecture using time-multiplexing. The proposed pTiBM block is initialized by four independent syndrome values during 4 clock cycles as shown in Fig. 6(b).

III. Result and Comparison

The proposed 16-channel time-multiplexing RS-based FEC architecture and conventional architectures\(^5\left[5\right]\)\(^6\left[6\right]\) were modeled in Verilog HDL and simulated to verify their functionality. It was then synthesized using appropriate time and area constraints. Both simulation and synthesis steps were carried out using SYNOPSYS design tools and 90-nm CMOS technology optimized. The conventional RS decoders in\(^5\left[5\right]\)\(^6\left[6\right]\) were synthesized using the same 90-nm CMOS technology. Table 1 shows the implementation results of the proposed 16-channel time-multiplexing RS-based FEC architecture and the other existing architectures. The total number of gates for the proposed architecture is 417,600 from the synthesized results (excluding the FIFO) and the clock frequency is 625 MHz. The proposed time-multiplexing architecture has higher throughput rate and lower hardware complexity than the parallel architectures in\(^5\left[5\right]\)\(^6\left[6\right]\).
This paper presented a high-speed, low-complexity VLSI architecture of 16-channel time-multiplexing RS-based FEC for next generation short-reach optical communication applications. A high-speed and high-throughput rate is facilitated by employing a three-parallel processing pipelining technique and modified syndrome computation block. The time-multiplexing method for resource sharing of pTiBM architecture is used in the parallel RS decoder to reduce hardware complexity. As a result, the proposed RS-based FEC architecture has a much higher throughput rate and lower hardware complexity compare to conventional architectures.

The proposed architecture has potential applications in RS-based FEC devices for short-reach optical communications with a data rate of 100 Gb/s and beyond.

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### IV. Conclusions

Table 1. Implementation results of the 16-channel RS-FEC.

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<td>192</td>
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### References