Parallel Architecture for Concatenated Polar-CRC Codes

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Abstract—This paper presents a parallel encoding and decoding method using concatenated polar-CRC codes to get high data throughput. Based on the proposed method, parallel architecture for concatenated polar-CRC codes is proposed. The proposed parallel concatenated polar-CRC decoding has better BER performance compared to conventional SC polar decoding without performance degradation in 3 dB SNR region.

Keywords— Polar codes; CRC codes; successive cancellation decoding; concatenated codes; architecture

I. INTRODUCTION

In binary-input memoryless channel (B-DMC), polar codes [1] can achieve the channel capacity under the assumption that the length of the code is enough long. Also, when compared with low-density parity-check (LDPC) codes or turbo codes, polar codes have an advantage that it has less decoding complexity [2]. Polar codes and LDPC codes have been accepted in 5G communication standards (3GPP) by as channel coding schemes for control and data channels, respectively. Polar codes have a low computational complexity and a simple structure compared with other channel codes. The first algorithm proposed by Arikan is the successive-cancellation (SC) algorithm [1]. Then, belief propagation (BP) algorithm [3] and SCL algorithm, which is an SC algorithm using the List decoding [4], have been proposed. Recently, it has been found that the SCL decoding method has higher error correction capability than LDPC codes and turbo codes, but it has a disadvantage that the latency is still long [2].

In this paper, we propose a novel parallel SC polar encoding and decoding methods by using short length codeword and using concatenated polar-cyclic redundancy check (CRC) codes.

II. PROPOSED PARALLEL CONCATENATED POLAR-CRC ENCODING AND DECODING

A. Proposed Encoding Method

As the code length increases, the latency required for the decoding process increases in the conventional SC polar decoder architecture. In [5], the pre-computation look-ahead SC polar decoder architecture was proposed to reduce the latency. The pre-computation look-ahead SC polar decoder is a structure that reduces the latency in the decoding process by pre-computes the calculation result of processing elements. When the length of the codeword is N, the decoding latency of the pre-computation look-ahead SC polar decoder is (N-1) clock cycles. As the length of the codeword N increases, the decoding latency, required in the decoding process, increases. The increase of the decoding latency is the major challenges for improvement of data throughput in the decoder design.

The proposed concatenated polar-CRC decoding method divides codeword and performs decoding process using sub-decoder with short length codeword. So, the proposed SC polar decoder reduces the decoding latency and improves data throughput. In order to compensate for the performance degradation caused by using the sub-decoders, a CRC code is concatenated with polar code. The performance degradation of the polar decoder is compensated by confirming whether the decoded code is error-corrected or not, and performing retransmission.

Fig. 1 shows a proposed parallel concatenated polar-CRC encoding and decoding method. The codeword length N of the proposed parallel SC code is 1024-bits, and the length of the information bits k is 512-bits, that is the code rate (k/N) is 0.5. Fig. 2 shows the proposed parallel concatenated polar-CRC encoding method. 512-bits input data is divided into four parts by 128-bits data for parallel processing. Divided 128-bits data is then passed through 8-bits CRC encoders to generate 8-bits CRC codes. (256, 136) polar encoders generate a 256-bits codeword with 136-bits of information bits obtained by concatenating 128-bits original data and 8-bits CRC codes. Then, a 1024-bits codeword including four 256-bits codewords is transmitted through the channel.

This work was supported by the Basic Science Research Program through the NRF funded by the Ministry of Science, ICT and Future Planning (2016R1A2B4015421), and supported by WCSL research grant directed by Inha University.
B. Proposed Decoding Method

The 1024 number of LLR values received over the channel are divided into four 256 LLR values for parallel processing. The four divided LLR values are input to four sub-decoders respectively. Then, (256, 136) SC polar sub-decoders decode 256-bits codeword. When the decoding step is completed, 136-bits of information bits excluding the frozen bits are separated from the 256-bits codeword. The separated 136-bits can be separated into 128-bits information bits and 8-bits CRC codes. And CRC decoder generates 8-bits CRC codes from 128-bits of information bits. The CRC codes generated at the receiving end is compared with the CRC codes transmitted at the transmitting end. Then, the decoder determines whether an error has occurred in the received data or not. If an error occurs in at least one sub-decoder, the codeword is retransmitted through the transmitter and the decoding process is performed again.

III. RESULTS AND COMPARISON

Fig. 3 shows BER performance of the proposed parallel concatenated polar-CRC polar decoding. The BER performance at the same Eb/N0 value is compared considering the retransmission. Especially, when the value of Eb/N0 value is 3dB or more, it can be confirmed that almost no retransmission occurs. When the value of Eb/N0 value is smaller than 3dB, many retransmissions occur and more energy is used in the transmission. Compared with the same Eb/N0 condition, it has low BER performance in the low Eb/N0 region due to the retransmission is occurred frequently. However, when the Eb/N0 value is more than 3 dB, the retransmission rarely occurs. In that case, the proposed parallel concatenated polar-CRC decoding has better BER performance compared with the conventional (1024, 512) SC polar decoders.

IV. CONCLUSIONS

In this paper, we propose a parallel concatenated polar-CRC encoding and decoding method with high data throughput. The proposed parallel concatenated polar-CRC decoding divides the codeword and performs decoding by using the sub-decoder. This method significantly reduces the decoding latency and improves data throughput.

REFERENCES